

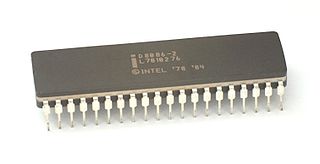
**Register Organization of Intel® 8086 vs. Intel® Pentium® 4 64-bit**

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**By Subhajit Sahu (110EC0181)**

**Under the Guidance of Prof. Sarat Kumar Patra**

**Department of Electronics and Communication National Institute of Technology, Rourkela**

**Register Organization of Intel® 8086**

BX (16b)

BL (8b)

BH (8b)

AX (16b)

AL (8b)

AH (8b)

**General Purpose Registers**

DL (8b)

DX (16b)

DH (8b)

CX (16b)

CL (8b)

CH (8b)

DI (16b)

SI (16b)

SP (16b)

BP (16b)

**Index Registers**

IP (16b)

ES (16b)

DS (16b)

SS (16b)

CS (16b)

**Segment Registers**

**Status / Flag Register**

C

-

P

-

A

-

Z

S

T

I

D

O

-

-

-

-

FLAGS (16b)

AX = Primary accumulator BX = Base, accumulator CX = Counter, accumulator DX = Data, accumulator

SI = Source Index DI = Destination Index BP = Base Pointer SP = Stack Pointer IP = Instruction Pointer

CS = Code Segment SS = Stack Segment DS = Data Segment ES = Extra Segment

FLAGS = Status / Flag Register

CS : IP 🡪 Memory address to next instruction to be executed SS : SP 🡪 Memory address last data stored on stack

**Register Organization of Intel® Pentium® 4 64-bit**

**General Purpose Registers**

AH

AL

AX (16b)

EAX (32b)

RAX (64b)

(8b)

(8b)

BH

BL

BX (16b)

EBX (32b)

RBX (64b)

(8b)

(8b)

CH

CX (16b)

ECX (32b)

RCX (64b)

(8b)

(8b)

CL

DH

DL

DX (16b)

EDX (32b)

RDX (64b)

(8b)

(8b)

**x = 8 🡪 15**

* **8 Registers**

RxL

RxW (16b)

RxD (32b)

Rx (64b)

(8b)

**Index Registers**

SIL

SI (16b)

ESI (32b)

RSI (64b)

(8b)

DIL

DI (16b)

EDI (32b)

RDI (64b)

(8b)

BPL

BP (16b)

EBP (32b)

RBP (64b)

(8b)

SPL

SP (16b)

ESP (32b)

RSP (64b)

(8b)

IP (16b)

EIP (32b)

RIP (64b)

**Segment Registers**

ES (16b)

DS (16b)

SS (16b)

CS (16b)

GS (16b)

FS (16b)

**Status / Flag Register**

FLAGS (16b)

EFLAGS (32b)

RFLAGS (64b)

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**FPU Registers**

**x = 0 🡪 7**

* **8 Registers**

STx (80b)

Status (16b)

Control (16b)

Opcode (11b)

Tag (16b)

Instruction Pointer (64b)

Data Pointer (64b)

**MMX Registers**

MMx (64b)

**x = 0 🡪 7**

* **8 Registers**

**XMM Registers**

XMMx (128b)

**x = 0 🡪 15**

* **8 Registers**

MXCSR (32b)

FPU 🡪 Floating Point Unit MMX 🡪 Single Instruction – Multiple Data Instruction Set XMM 🡪 Streaming SIMD Instruction Set

**Register Organization of different Register Types**

General Purpose Registers:

These registers are used for arithmetic operations and temporary storage. BX / RBX / RCX can also be used for memory indexing for read/write.

Index Registers:

These registers are normally used for indexing memory for read/write. IP / RIP is a special register which stores the address of the next instruction to be executed.

Segment Registers:

These registers are used for segmentation operation in memory. These were very importantly used in 8086, but their usage is much reduced now due to flat memory concept, which is currently in use.

Flag Register:

This register stores the status of the last arithmetic operation, along with much more other boolean information, which indicate the state of the processor.

FPU Registers:

These are Floating Point Unit registers, used for performing floating-point arithmetic operations.

MMX Registers:

These are special purpose registers, used for Single Instruction – Multiple Data (SIMD) instructions which help improve processing speed for large volume data processing applications.

XMM Registers:

These are special purpose registers, used for Streaming SIMD instructions (SSE) which help improve processing speed for large volume data processing applications.

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